PSEUDO RANDOM OPTIMIZED BUILT-IN SELF-TEST

ABSTRACT

Flat pseudo random test patterns are provided in combination with weighted pseudo random test patterns so that the weight applied to every latch in a LSSD shift register (SR) chain can be changed on every cycle. This enables integration of on-chip weighted pattern generation with either internal or external weight set selection. WRP patterns are generated by a tester either externally or internally to a device under test (DUT) and loaded via the shift register inputs (SRIs or WPIs) into the chip's shift register latches (SRLs). A test (or LSSD tester loop sequence) includes loading the SRLs in the SR chains with a WRP, pulsing the appropriate clocks, and unloading the responses captured in the SRLs into the multiple input signature register (MISR). Each test can then be applied multiple times for each weight set, with the weight-set assigning a weight factor or probability to each SRL.